REMARKS

The Examiner indicates that claims 27-38 are allowable over the prior art, provided that the 35 U.S.C. § 112, first paragraph rejection of the same claims can be overcome.

Reconsideration of the Section 112, first paragraph rejection is respectfully requested for the following reasons. The Examiner indicates that the only notable disclosure of the predetermined error state patterns is on page 8, lines 14-16 indicating that the error states are evaluated by the coordination module where they are stored and compared with predetermined error patterns. However, there are additional disclosures in the specification which, when coupled with the above disclosure, clearly indicate that both the received and stored error patterns, and the predetermined stored error patterns for comparison, are of the same type. First, it is clear and logical to one skilled in this art reading this specification that in order to compare "apples to apples" that the predetermined error pattern for comparison must be of the same type as the received error pattern. It is very clear from Fig. 2 that the received error pattern is a plurality of error states at predetermined time points. Thus the stored predetermined error pattern must also be error states at predetermined time points. Otherwise no effective comparison could be made.

Secondly, and even more importantly, note the disclosure in the substitute specification at page 4, lines 17-18 stating that with the aid of preset error patterns, an exact evaluation of the error cause by the controller can occur. Such an "exact" evaluation could logically only be provided where the stored predetermined error pattern is of the same nature and type (comparison of apples to apples) as the received error pattern shown in Fig. 2. Also see page 7, lines 13-15 stating that an error storage, in which error statistics and operation states are stored and protocoled

in the temporal sequence of their occurrence, is also contained in the controller 14. This temporal sequence of their occurrence is clearly referring to both the received error pattern and the predetermined error pattern for comparison.

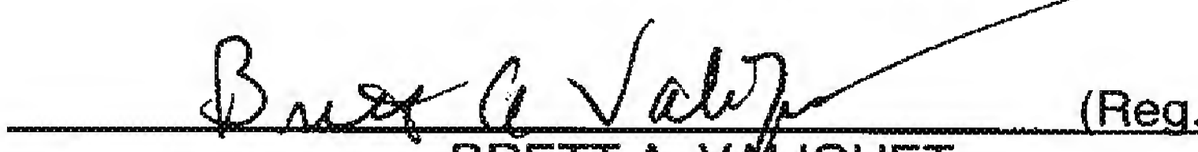
Next note page 8, lines 14-20 stating that the error states transmitted as shown in Fig. 2 are stored and compared with predetermined error patterns. This indicates that the transmitted error states in Fig. 2 in the time span T are evaluated with respect to the predetermined error patterns. And note at line 17 that the specification states that the error patterns contain one or more error states, whereby given a plurality of error states the sequence of their occurrence and/or the sequence of their notification to the controller 14 is also taken into account. Note that the term "error patterns" is plural, and thus is referring to both a received error pattern and a stored error pattern when discussing the sequence of their occurrence and sequence of their notification.

Finally, the specification at page 8, lines 21-27 states: "In the present exemplary embodiment, a recording error is registered at the coordination module CM at the point in time t3 and a paper flow error is registered at the coordination module CM at the point in time t4. This (emphasis added) error pattern indicates that the first registered recording error is a consequent error of the subsequently (emphasis added) registered paper flow error. The coordination module CM thus determines the paper flow error using the stored error pattern as a "causative error and registers this to the controller 14." Thus the specification is here clearly disclosing that the predetermined error pattern is recognizing both the recording error at time t3 and a paper flow error at time t4 since it determines that one error is subsequent to the other. This is thus clearly a teaching that the predetermined error pattern compares both the error states and the time points.

From all of the above disclosures taken in combination, and particularly the last disclosure mentioned at page 8, lines 21-27, one skilled in the art understands that the specification is disclosing that the predetermined error pattern compared to the received error pattern is a comparison of both error state and time sequence (temporal sequence). This permits, in the words of applicant's specification, "an exact evaluation of the error cause by the controller" – specification page 4, line 17.

Reconsideration is respectfully requested in view of the above.

Respectfully Submitted



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The Commissioner is hereby authorized to change any additional fees which may be required, or to credit any overpayment to Account No. 501519.

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